REMARKS

Applicant wishes to thank the Examiner for the consideration given the present application. The Examiner's Office Action of **August 15, 2001,** has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a Three (3) Month Extension of Time* that extends the statutory period for response to **February 15, 2001**. Accordingly, Applicant respectfully submits that this response is timely filed and fully response to the Office Action.

Claims 78-157 were pending in this application prior to the aforementioned amendment. By the above amendments, claims 78, 79, 84, 90, 91, 96, 97, 102, 109, 110, 117, 118, 121, 126, 129, 134, 135, 140, 141, 146, 151, 152, and 157 are amended in order to place the invention in condition for allowance. Applicant asserts that no issue of new matter is set forth by the above amendments. Accordingly, claims 78-157 are still pending in this application, and are believed to be in condition for allowance at least for the reasons stated below.

A. 35 U.S.C. §103 Rejections

The Office Action rejects claims 78, 80, 84, 86, and 89 under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 4,755,865 to ***Wilson et al.*** (Hereinafter "***Wilson***"), claims 78-101, 110-115, 117-127, 129-138 and 146-157 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of U.S. Patent No. 4,772,927 to ***Saito et al.*** (Hereinafter "***Saito***") and U.S. Patent No. 4,841,348 to ***Shizukuishi et al.*** (Hereinafter "***Shizukuishi***"), claim 116 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of ***Saito***, ***Shizukuishi*** and U.S. Patent No. 5,219,784 to ***Solheim***, claims 128 and 139 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of ***Saito*** and U.S. Patent No. 4,694,317 to ***Higashi***, claims 102-107, 109 and 140-144 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of ***Saito***, ***Shizukuishi***

and U.S. Patent No. 4,766,471 to ***Ovshinsky et al.*** (Hereinafter "***Ovshinsky***"), claim 145 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of ***Saito***, ***Shizukuishi***, ***Ovshinsky*** and ***Higashi***, and claim 108 under 35 U.S.C. 103(a) as unpatentable over ***Wilson*** in view of ***Saito***, ***Shizukuishi***, ***Ovshinsky*** and ***Solheim***. Applicant respectfully contends that the claimed invention as presently amended defines subject matter which Applicant believes is patentably distinct over the prior art for at least the reasons that follow.

It should be noted that three criteria must be met to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

As presently amended, the claimed invention is directed generally to a semiconductor device including, *inter alia*, a semiconductor layer including a channel region and source and drain regions in contact with the channel region at a source-channel boundary and a drain-channel boundary, respectively, a region formed in the vicinity of at least one of the source-channel boundary and the drain-channel boundary in the semiconductor layer, the region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen. In accordance with an exemplary embodiment of the claimed invention, one boundary of the region including is located within the channel region.

Applicant respectfully contends that the ***Wilson*** patent, either alone or in combination with the ***Saito***, ***Shizukuishi***, ***Solheim***, ***Higashi***, or ***Ovshinsky*** patents, fails to expressly teach

or implicitly suggest every limitation of the claimed invention necessary to support *prima facie* obviousness under 35 U.S.C. §103(a).

Referring now to the Office Action, in which the Examiner finds that the base reference, i.e., the ***Wilson*** patent, teaches the subject invention substantially as claimed. In Applicant's review of the express disclosure of the ***Wilson*** patent, however, it appears that the ***Wilson*** patent merely discloses a region 42C in a semiconductor layer that contains nitrogen or oxygen that are located in source and drain regions (See Fig. 3). In contradistinction thereto, and in accordance with at least amended claims 78 and 84 of the claimed invention, the semiconductor device includes a region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen, wherein one boundary of the region is located within the channel region. Thus, the ***Wilson*** patent is deficient as a base reference since it fails to expressly teach or implicitly suggests that one boundary of the nitrogen or oxygen region is formed in the channel region.

The Examiner also finds that, although the ***Wilson*** patent fails to expressly disclose a region of oxygen overlapping a portion of the channel region, the ***Wilson*** patent does disclose at column 4, lines 56-59 that the oxygen migrates into the channel region. The Examiner further finds that the ***Saito*** patent points out the advantages of using a TFT having source and drain regions containing carbon, nitrogen, or oxygen at a concentration higher than 10E19 atoms per cm cube or more in a CMOS device, while the ***Shizukuishi*** patent discloses a MOS transistor being used in a CMOS device which is part of a peripheral circuit of an active matrix type device having of pixels.

It seems that the ***Wilson*** patent, however, considers that the oxygen does not migrate into the channel region and that it is unnecessary to regard the oxygen immigration in view of the express disclosure on column 4, lines 56-59. Accordingly, Applicant respectfully contends that the ***Wilson*** patent fails to disclose that one boundary of the region is located

within the channel region, and thus, the claimed invention is not obvious in view of the express teaching of the ***Wilson*** patent.

With respect to the ***Saito*** patent, carbon, nitrogen, or oxygen is introduced through the whole area of the channel region and the source and drain regions in order to restrain the conductive impurity in the source and drain regions from diffusing into the channel region. Accordingly, the ***Saito*** patent fails to suggest that the region having carbon, nitrogen, or oxygen is established at an area in which an electric field concentrates, that is, only at the vicinity of the drain-channel boundary.

On the other hand, in accordance with the claimed invention, the region yields non-obvious advantageous benefits not seen n the prior art since it permits the establishment of a high band gap which is capable of avoiding leakage of the carriers. This is accomplished by providing the region at an area in which an electric field concentrates, e.g., at the vicinity of the drain-channel boundary. Due to the claimed structure, it is possible to prevent the occurrence of a reverse current leakage from the drain region to channel region since the carriers cannot migrate to the channel region due to the large band gap of the region. See FIG. 10. Furthermore, it is possible to elevate the drain voltage resistance since a potential barrier can be established by increasing the band gap at the region. Since the ***Saito*** patent fails to suggest a region having carbon, nitrogen, or oxygen being established at an area in which an electric field concentrates, the benefits derived from the claimed invention cannot be achieved. Therefore, there is a lack of motivation to compel one of ordinary skill in the art to combine the respective teachings of the ***Wilson*** and ***Saito*** patents in order to arrive at the claimed invention.

The ***Solheim*** patent is relied upon to show a threshold voltage of a NMOS being approximately equivalent to that of the PMOS, the ***Higashi*** patent is relied upon to show a transparent or a reflective device comprising a first interlayer insulating film comprising

inorganic material, a second ILD film comprising organic resin and a pixel electrode on the second ILD film, and the ***Ovshinsky*** patent is relied upon to show an element comprising carbon can widen the band gap in a silicon layer containing elements such as germanium or boron. However, in view of the lack of motivation to combine the ***Wilson*** and ***Saito*** patents as mentioned hereinabove, even if the ***Solheim***, ***Higashi***, or ***Ovshinsky*** patents are combined thereto, it would not produce a device that would render the claimed invention obvious under §103.

For at least the above reasons, it is respectively asserted that claims 78-157 are now in proper condition for allowance and reconsideration of the pending rejections is respectively requested. If the Examiner believes that any further discussions would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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Marked-up copy of amended claims.

78. (Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein [said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary] one boundary of said region is located within the channel region and the other boundary is located within one of the source region and said drain region.

79. (Amended) A device according to claim 78 wherein said semiconductor [device has transistors] layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

84. (Amended) A semiconductor device comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary and one boundary of said region is located within the channel region.

90. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary and one boundary of said region is located within the channel region.

91. (Amended) A device according to claim 90 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

96. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions in contact with said channel region at a source-channel boundary and a drain-channel boundary, respectively;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions,

wherein said region is formed in the vicinity of at least one of said source-channel boundary and said drain-channel boundary and one boundary of said region is located within the channel region.

97. (Amended) A device according to claim 96 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

102. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and the other boundary is located within one of the source region and said drain region.

109. (Amended) A device according to claim 102 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

110. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and the other boundary is located within one of the source region and said drain region.

117. (Amended) A device according to claim 110 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

118. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels; and

at least one driver circuit for driving said pixels formed over the substrate, said driver circuit comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and the other boundary is located within one of the source region and said drain region.

121. (Amended) A device according to claim 118 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

126. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in said semiconductor layer, said region containing one or more elements selected from the group consisting of carbon, nitrogen, and oxygen at a concentration of 1×10^{19} atoms/cm^3 or more, wherein one boundary of said region is [formed

in] located within said channel region [and the other boundary of said region is formed in one of said source region and said drain region].

129. (Amended) A device according to claim 126 wherein said [device comprises transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

134. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween;

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween; and

a region having a higher energy band gap than any of said source, drain, and channel regions, said region formed in the vicinity of at least one of a source-channel boundary and a drain-channel boundary in the semiconductor layer,

wherein one boundary of said region is [formed in] located within said channel region [and the other boundary of said region is formed in one of said source region and said drain region].

135. (Amended) A device according to claim 134 wherein said [display device comprises transistors] semiconductor layer is an active layer of a thin film transistor selected

from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

140. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween,

wherein said semiconductor layer has at least one region including carbon and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including carbon is located within the channel region and the other boundary is located within one of the source region and said drain region.

141. (Amended) A device according to claim 140 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.

146. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including nitrogen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including nitrogen is located within the channel region and the other boundary is located within one of the source region and said drain region.

151. (Amended) A device according to claim 146 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors..

152. (Amended) A [display] semiconductor device [having] comprising:

a pixel portion formed over an substrate, said pixel portion comprising a plurality of pixels, each of said pixels comprising:

a semiconductor layer including a channel region and source and drain regions with said channel region interposed therebetween; and

a gate electrode adjacent to said channel region with a gate insulating film interposed therebetween;

wherein said semiconductor layer has at least one region including oxygen and overlapping both a portion of said channel region and a portion of said source and drain regions at concentration of 1×10^{19} atoms/cm^3 or more, and

wherein one boundary of said region including oxygen is located within the channel region and the other boundary is located within one of the source region and said drain region.

157. (Amended) A device according to claim 152 wherein said [display device has transistors] semiconductor layer is an active layer of a thin film transistor selected from the group consisting of stagger type, inverted stagger type, planar type, and inverted planar type transistors.